ARCHITECTURE FOR A FASTER MAX* COMPUTATION

ABSTRACT OF THE DISCLOSURE

An architecture for a turbo decoder performs a faster max* computation. In this architecture, one or more lookup tables begin processing a digital signal prior to the most significant bit of the digital signal stabilizes. This technique allows processing in the lookup table to be accomplished during a period of time in which processing could not be accomplished previously. As a result, the architecture performs the max* computations at a faster rate than previous architectures.